ALPHA & OMEGA SEMICONDUCTOR
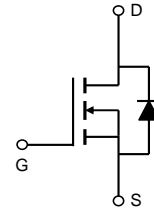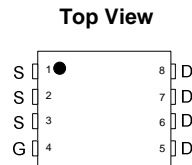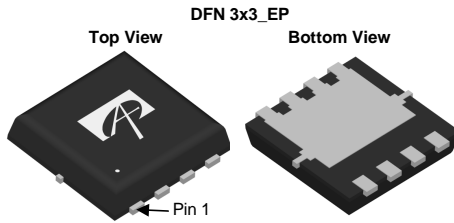
AON7446

60V N-Channel MOSFET
SDMOS™

General Description

The AON7446 is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge and low Qrr.The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

Product Summary

V_{DS}	60V
I_D (at V_{GS}=10V)	8A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 145mΩ
$R_{DS(ON)}$ (at V_{GS} = 7V)	< 160mΩ

100% UIS Tested
100% R_g Tested

Green Product

DFN 3x3_EP

Top View   **Bottom View**

← Pin 1

Top View

```
S [ 1•        8 ] D
S [ 2         7 ] D
S [ 3         6 ] D
G [ 4         5 ] D
```

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	8	A
	T_C=100°C		5	
Pulsed Drain Current [C]		I_{DM}	17	
Continuous Drain Current	T_A=25°C	I_{DSM}	3.3	A
	T_A=70°C		2.7	
Avalanche Current [C]		I_{AS}, I_{AR}	10	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	5	mJ
Power Dissipation [B]	T_C=25°C	P_D	16.7	W
	T_C=100°C		7	
Power Dissipation [A]	T_A=25°C	P_{DSM}	3.1	W
	T_A=70°C		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	30	40	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		60	75	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	6.2	7.5	°C/W

Electrical Characteristics (T$_J$=25℃ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250μA, V$_{GS}$=0V		60			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=60V, V$_{GS}$=0V				10	μA
			T$_J$=55℃			50	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$= ±20V				100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=V$_{GS}$ I$_D$=250μA		2.2	2.7	3.3	V
I$_{D(ON)}$	On state drain current	V$_{GS}$=10V, V$_{DS}$=5V		17			A
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=3A			113	145	mΩ
			T$_J$=125℃		197	237	
		V$_{GS}$=7V, I$_D$=2.5A			118	160	mΩ
g$_{FS}$	Forward Transconductance	V$_{DS}$=5V, I$_D$=3A			7.5		S
V$_{SD}$	Diode Forward Voltage	I$_S$=1A,V$_{GS}$=0V			0.76	1	V
I$_S$	Maximum Body-Diode Continuous Current					15	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=30V, f=1MHz		190	237	285	pF
C$_{oss}$	Output Capacitance			17	25	33	pF
C$_{rss}$	Reverse Transfer Capacitance			5	9	13	pF
R$_g$	Gate resistance	V$_{GS}$=0V, V$_{DS}$=0V, f=1MHz		0.7	1.4	2.1	Ω
SWITCHING PARAMETERS							
Q$_g$	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=30V, I$_D$=3A		3.5	4.4	5.3	nC
Q$_{gs}$	Gate Source Charge			0.7	0.9	1.1	nC
Q$_{gd}$	Gate Drain Charge			0.7	1.1	1.6	nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=30V, R$_L$=10Ω, R$_{GEN}$=3Ω			4.5		ns
t$_r$	Turn-On Rise Time				1.5		ns
t$_{D(off)}$	Turn-Off DelayTime				15		ns
t$_f$	Turn-Off Fall Time				1.5		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=3A, dI/dt=500A/μs		5.4	7.7	10	ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I$_F$=3A, dI/dt=500A/μs		9	13	17	nC

A. The value of R$_{θJA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$ =25℃. The Power dissipation P$_{DSM}$ is based on R $_{θJA}$ t ≤ 10s value and the maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design, and the maximum temperature of 150℃ may be u sed if the PCB allows it.

B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=150℃. Ratings are based on low frequency and duty cycles to keep initial T$_J$ =25℃.

D. The R$_{θJA}$ is the sum of the thermal impedance from junction to case R$_{θJC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T$_{J(MAX)}$=150℃. The SOA curve provides a single pulse ratin g.

G. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T$_A$=25℃.

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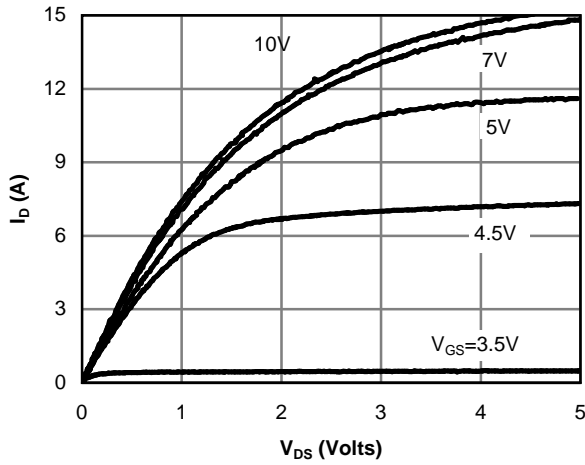
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

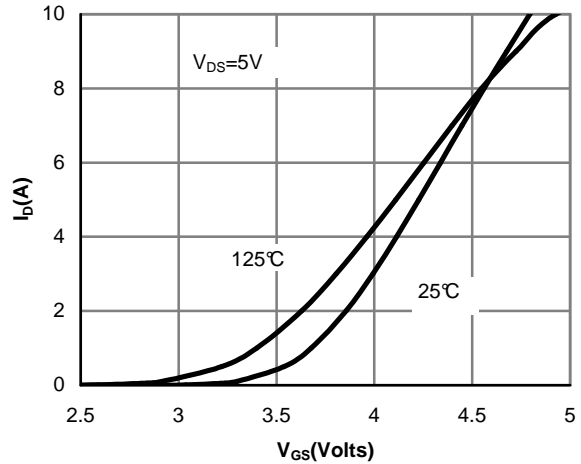Fig 1: On-Region Characteristics (Note E)
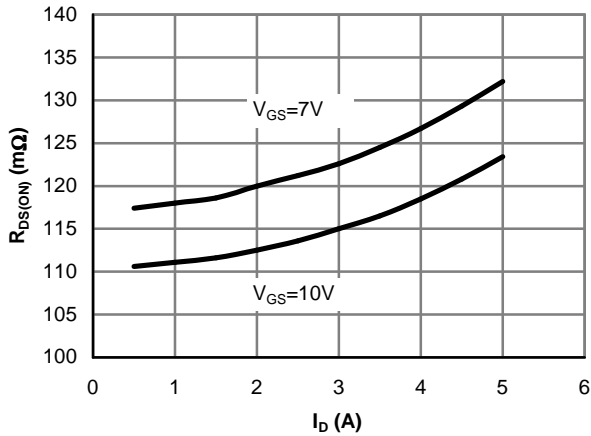
Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)
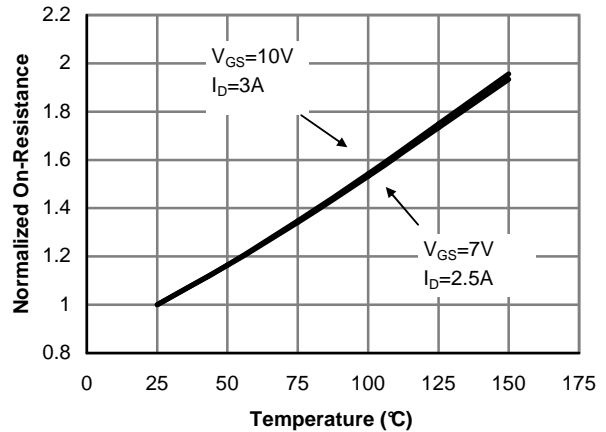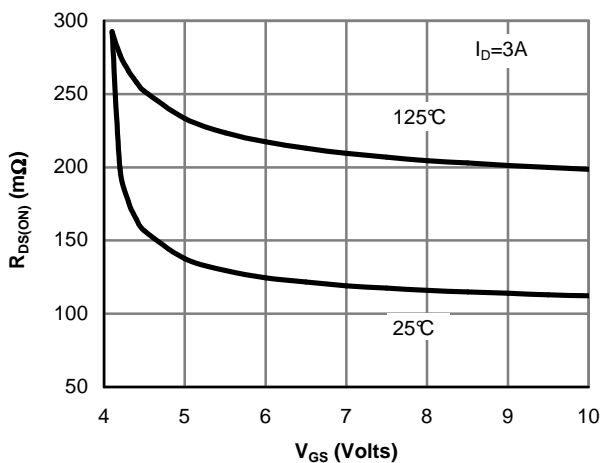
Figure 4: On-Resistance vs. Junction Temperature (Note E)

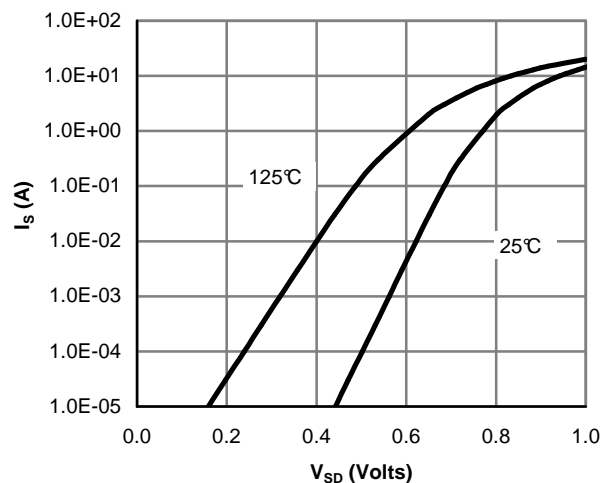Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

Figure 6: Body-Diode Characteristics (Note E)
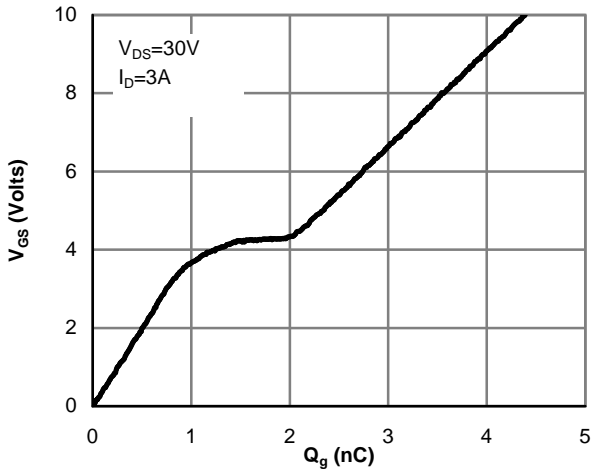
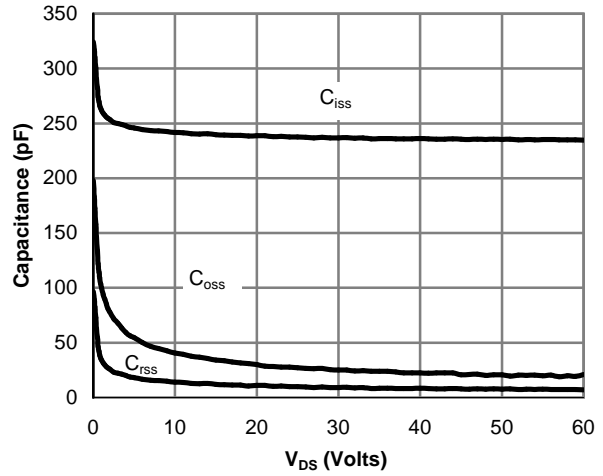## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 7: Gate-Charge Characteristics

Figure 8: Capacitance Characteristics
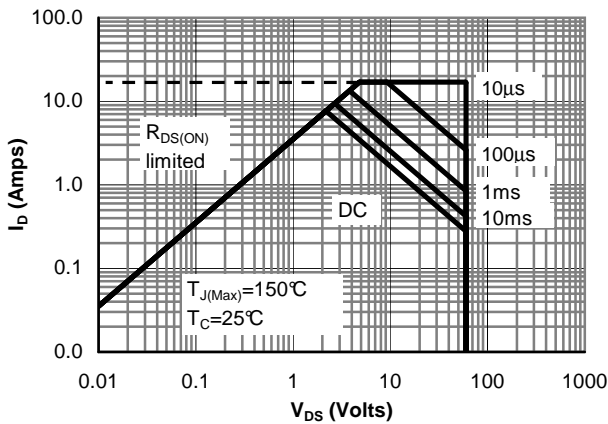
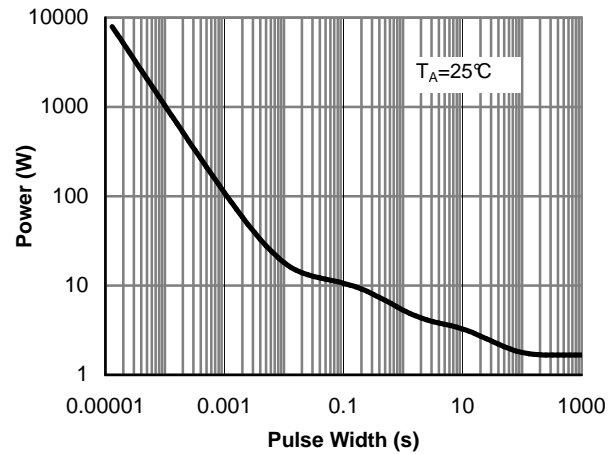Figure 9: Maximum Forward Biased Safe Operating Area (Note F)
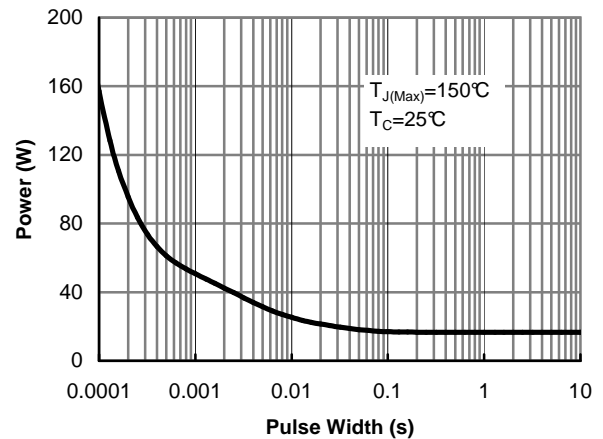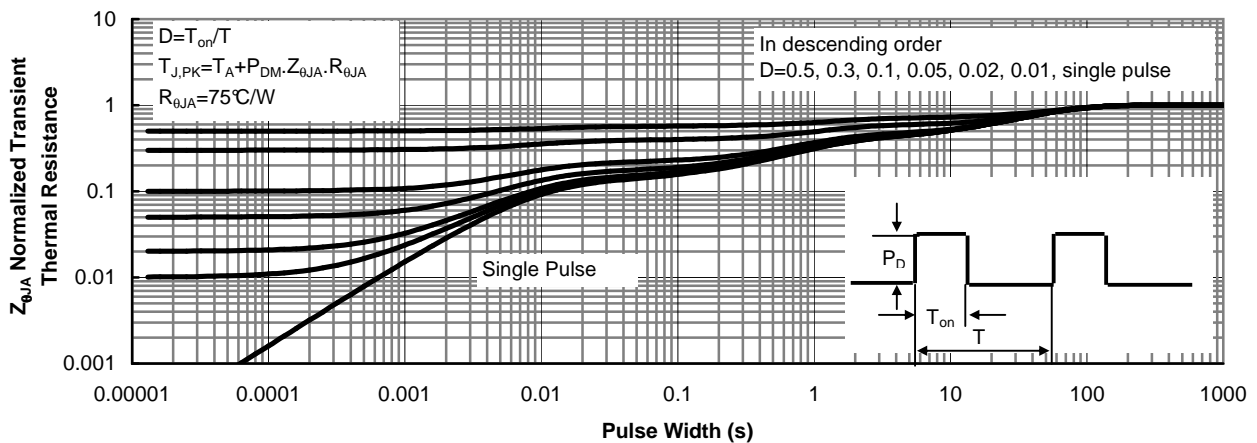

Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)
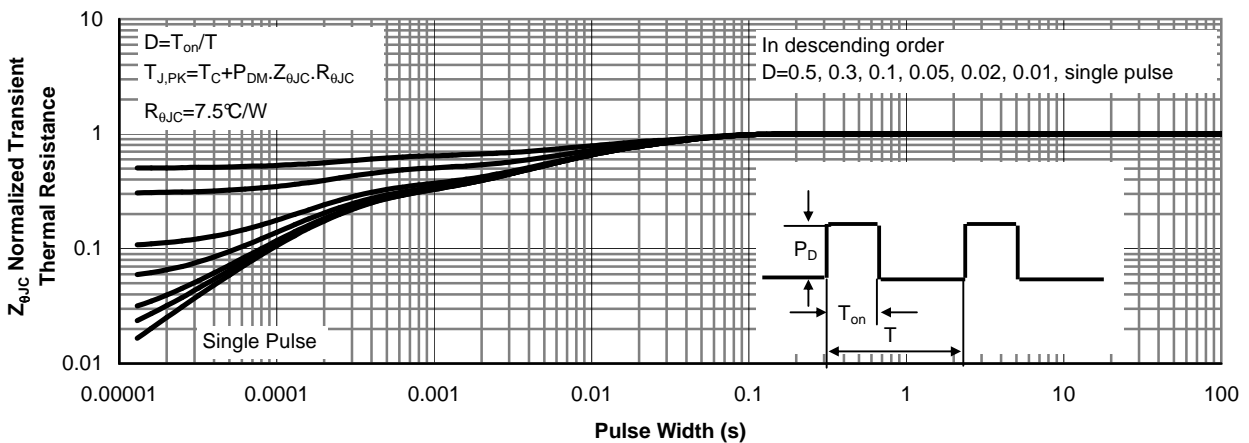
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
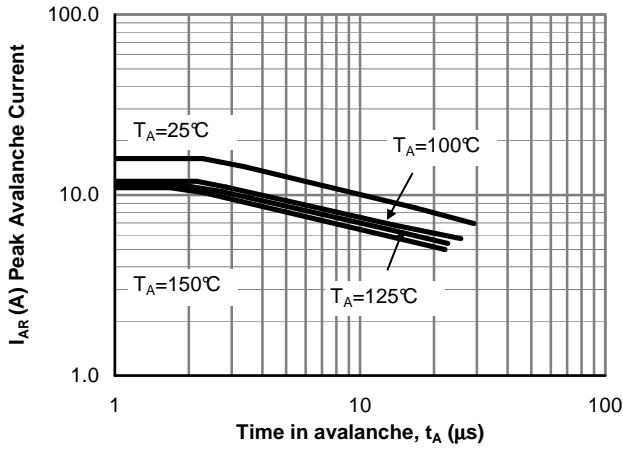
Figure 12: Single Pulse Avalanche capability (Note C)
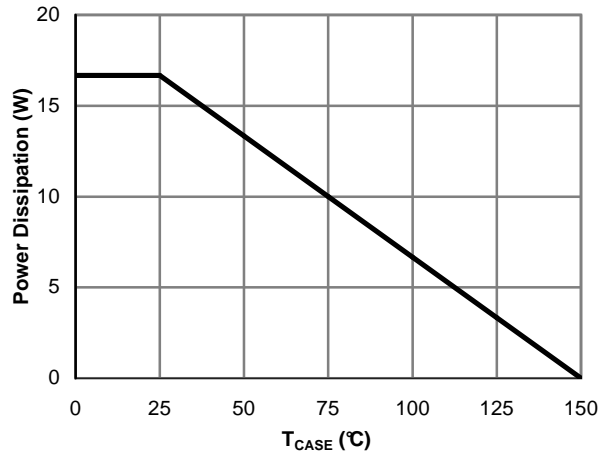
Figure 13: Power De-rating (Note F)
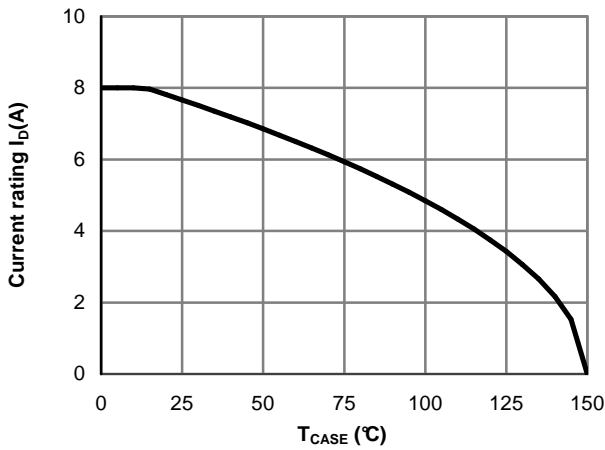
Figure 14: Current De-rating (Note F)

Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

$D=T_{on}/T$

$T_{J,PK}=T_A+P_{DM}\cdot Z_{\theta JA}\cdot R_{\theta JA}$

$R_{\theta JA}=75℃/W$

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse

Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
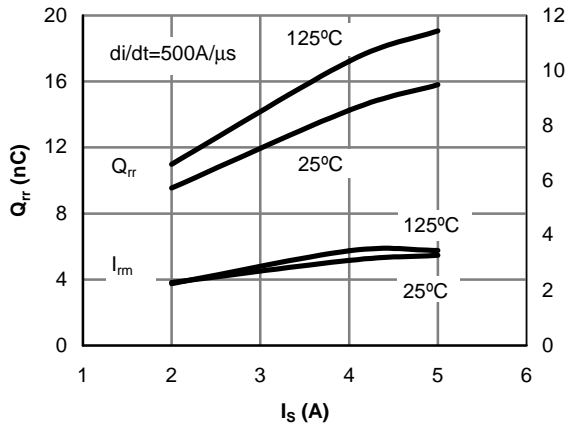
**Figure 17: Diode Reverse Recovery Charge and
Peak Current vs. Conduction Current**
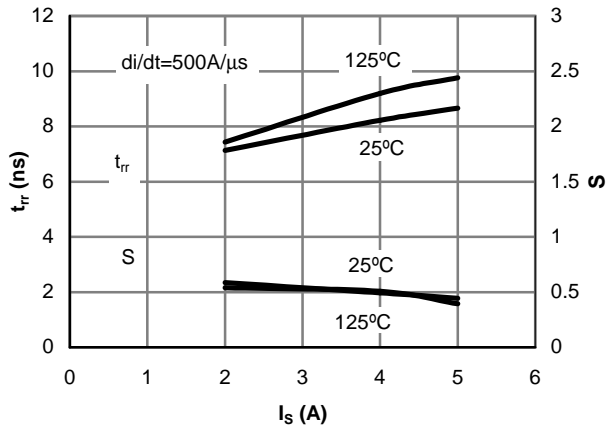
**Figure 18: Diode Reverse Recovery Time and
Softness Factor vs. Conduction Current**
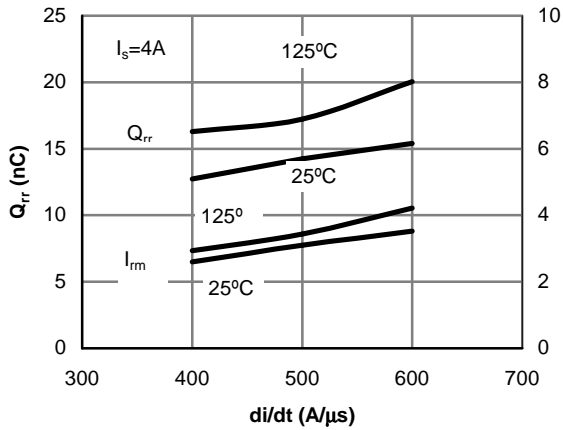
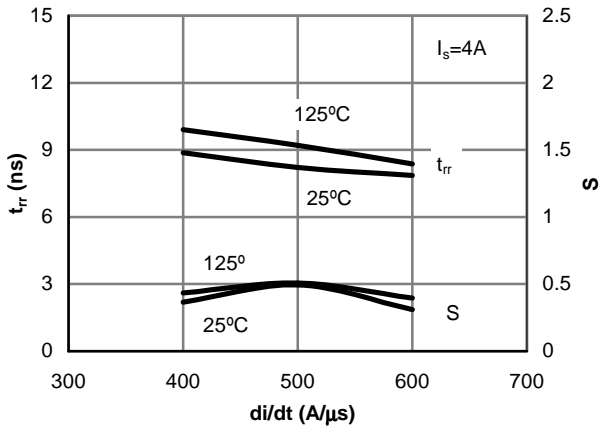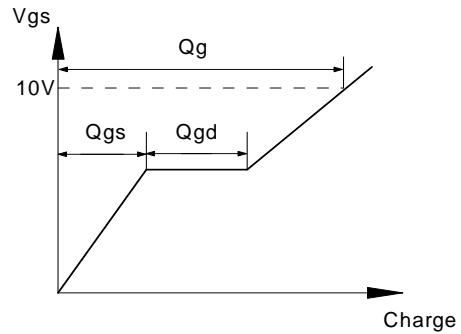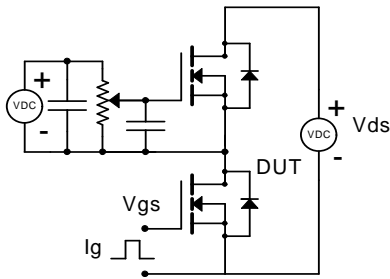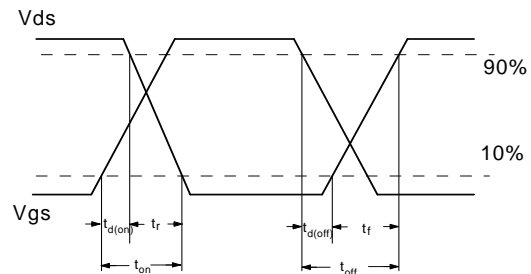**Figure 19: Diode Reverse Recovery Charge and
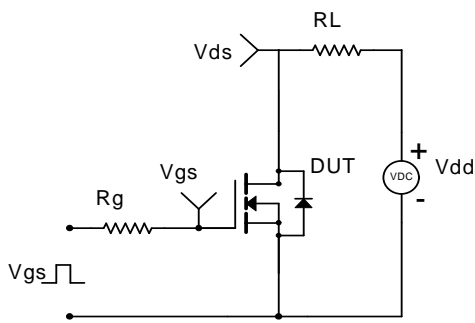Peak Current vs. di/dt**

**Figure 20: Diode Reverse Recovery Time and
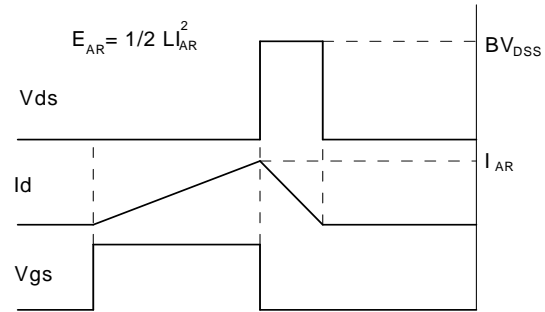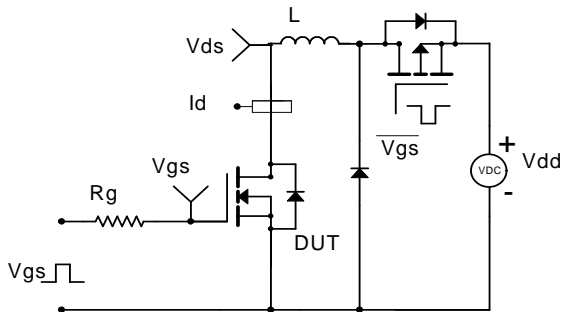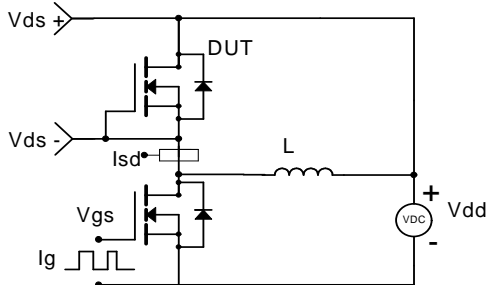Softness Factor vs. di/dt**

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2\, LI_{AR}^2$$

Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int Idt$$
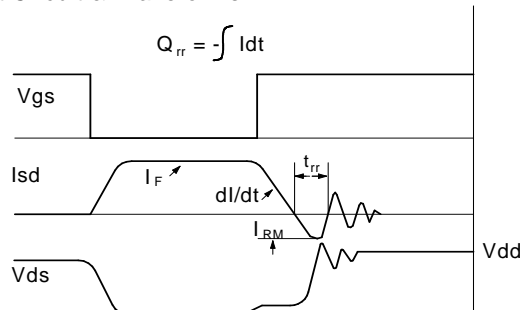
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